Claims 4, 10, 17, 24, 31, 38, and 45 have been amended to more clearly describe the scope of the claims in compliance with 35 USC § 112. Applicant respectfully submits that these claims as amended are in compliance with 35 USC § 112, first paragraph. Reconsideration and withdrawal of the rejection is respectfully requested.

§102 Rejection of the Claims

Claims 1, 2, 5, and 6 were rejected under 35 USC § 102(e) as being anticipated by Yu (U.S. 6,268,253).

Applicant does not admit that Yu is indeed prior art and reserves the right to swear behind this reference at a later date. Nevertheless the Applicant believes that the present invention is distinguishable from the reference for the following reasons.

The rejection states that:

Yu teaches a method of reducing a channel length in a transistor, comprising: forming a gate dielectric layer (204) on a semiconductor substrate (102); coupling a barrier layer (206) to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth; forming a gate (208) on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and an amount of overlap between the sides of the gate and a pair of source/drain regions (see fig. 7) and oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide (212) and an effective channel length of the gate is reduced (figs. 4 and 5).

Yu appears to show forming "a removable spacer 212 on the sidewalls of the gate structure 208." The removable spacer 212 of Yu appears to be "formed by using the gate material of the gate structure 208." (Col 5, lines 39-42). However, Applicant respectfully submits that Yu does not show oxidizing the gate **with sides of the gate dielectric exposed**, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

In contrast, Applicant's present application teaches a method where diffusion through exposed sides of the gate dielectric is controlled. Applicant's independent claim 1 as amended includes oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

Because the Yu reference does not show every element of Applicant's independent claim 1, a 35 USC § 102(e) rejection is not supported. Reconsideration and withdrawal of the rejection

is respectfully requested with respect to Applicant's independent claim 1. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Claims 7, 8, 14, 15, 18, 19, and 54 were rejected under 35 USC § 102(b) as being anticipated by Xiang et al. (U.S. 5,866,473).

The rejection states that:

Xiang teaches a method of forming transistor comprising: forming a first source/drain region (212) and a second source/drain region (216) in a semiconductor substrate (204); forming a gate dielectric layer (202) on a semiconductor substrate (204); coupling a barrier layer (206) to the gate dielectric layer wherein the barrier layer prevents oxide undergrowth; forming a gate (208) on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide (220) and an effective channel length of the gate is reduced (figs. 2A-2F).

Applicant assumes that selected elements in the Xiang rejection are typographically in error. For example, element 206 does not appear to be a barrier layer, and element 208 does not appear to be a gate. Applicant has attempted to infer the intent of the rejection, and distinguishes the reference as follows.

Xiang appears to show a gate oxide layer 202 that may include nitrogen (col. 2, lines 46-47). Xiang also appears to show oxidation of a portion of a polysilicon gate electrode 206 to reduce a dimension of the polysilicon gate 206. However, Xiang does not recognize the problem of diffusion from underneath a gate dielectric as discussed in Applicant's specification on page 2, lines 15-30. Further, Xiang does not show, teach or suggest oxidizing the gate **with sides of the gate dielectric exposed**, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

In contrast, Applicant's present application teaches a method where diffusion through exposed sides of the gate dielectric is controlled. Applicant's independent claims 7, 14, and 54 as amended each include oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

Because the Xiang reference does not show every element of Applicant's independent claims, a 35 USC § 102(b) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 7, 14, and 54. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

§103 Rejection of the Claims

Claims 3, 4, 9-10, 16-17, and 21-48 were rejected under 35 USC § 103(a) as being unpatentable using various combinations of references, each combination including the Yu reference or the Xiang reference.

Applicant respectfully submits that neither the Gardner reference, nor the Sung reference cures the deficiencies of Yu and Xiang as argued above. Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to claims 3, 4, 9-10, 16-17, and 21-48.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 21st day of January, 2003

Amy Moriarty
Name

Signature